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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/755,449	01/13/2004	Vladimir Vasekin	550-500	1088
23117	7590	04/19/2006		
NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203			EXAMINER GEIB, BENJAMIN P	
			ART UNIT	PAPER NUMBER
			2181	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/755,449		VASEKIN, VLADIMIR	
	<b>Examiner</b>		<b>Art Unit</b>	
	Benjamin P. Geib		2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 13 January 2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

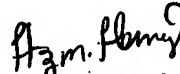
**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

  
**FRITZ FLEMING**  
**PRIMARY EXAMINER** 4/17/2006  
**GROUP 2100**  
**AU 2181**

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>1/13/2004, 8/12/2004, 4/13/2004</u>                                       | 6) <input type="checkbox"/> Other: _____                                    |

### DETAILED ACTION

1. Claims 1-30 have been examined.
2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 01/13/2004, Information Disclosure Statement on 08/12/2004, and Information Disclosure Statement on 09/13/2004.

### *Priority*

3. Receipt of papers submitted under 35 U.S.C. 119(a)-(d) is acknowledged; the papers have been placed on record in the file. The certified copy of 0307821.9, filed on 04/04/2003 has been received and placed on record.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:  

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claims 9, 19 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
6. Claim 9 recites the limitation "wherein said exception handling circuit is operable" in line 2. Since there is no previous mention of an exception handling circuit, there is insufficient antecedent basis for this limitation in the claim. The limitation will be interpreted as "comprising an exception handling circuit operable" for the remainder of the examination.

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7. Claims 9, 19, and 29 recite the limitation "said address of said execute block instruction" in lines 2-3. Since there is no previous mention of an address for the said execute block instruction, there is insufficient antecedent basis for this limitation in the claim. The limitation will be interpreted as "an address of said execute block instruction" for the remainder of the examination.

8. Claims 19 and 29 recite the limitation "upon occurrence of said exception" in line 2. Since there is no previous mention of an exception within the claims, there is insufficient antecedent basis for this limitation in the claim. The limitation will be interpreted as "upon occurrence of an exception" for the remainder of the examination.

***Claim Rejections - 35 USC § 101***

9. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 21-29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 21 refers to "a computer program product", which is defined within the specification as including "a storage medium bearing the computer program or a download or transmission of a computer program" (page 7, first full paragraph). This definition includes transmission media, which is non-statutory subject matter.

***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-7, 10-17, 20-27, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Fraser, U.S. Patent No. 6,907,598.

13. Referring to claim 1, Fraser has taught an apparatus for processing data, said apparatus comprising:

an instruction fetching circuit [*access module; Fig. 3, component 332*] operable to fetch program instructions from a sequence of memory locations [*column 11, line 65 – column 12, line 3*];

an instruction decoder [*evaluate module; Fig. 3, component 334*] responsive to program instructions fetched by said instruction fetching circuit to control data processing operations specified by said program instructions [*column 12, lines 3-13*];  
and

an execution circuit [*execute module; Fig. 3, component 338*] operable under control of said instruction decoder to execute said data processing operations [*column 12, lines 7-13*];

wherein said instruction decoder is responsive to an execute block instruction *[echo instruction]* to trigger fetching of a block of two or more program instructions *[set of instructions]* by said instruction fetching circuit and execution of said block of two or more program instructions by said execution circuit, said block of two or more instructions containing a number of program instructions specified by a block length field *[length parameter]* within said executed block instruction and being stored at a memory location specified by a location field *[displacement parameter]* within said execute block instruction *[When the evaluate module determines there is an echo instruction it triggers the fetching and execution of a set of instructions, whose number and location are indicated by the length and displacement parameters, respectively, of the echo instruction; column 12, lines 14-44].*

14. Referring to claim 2, Fraser has taught the apparatus as claimed in claim 1, wherein after execution of said block of two or more program instructions a return is made to a program instruction outside of said block of two or more program instructions *[column 12, lines 32-44].*

15. Referring to claim 3, Fraser has taught the apparatus as claimed in claim 1, wherein said return is to a program instruction immediately following said execute block instruction within said sequence of memory locations *[column 12, lines 32-44].*

16. Referring to claim 4, Fraser has taught the apparatus as claimed in claim 1, wherein said location field is an offset field *[displacement parameter]* specifying said location of said block of two or more program instructions relative to a memory location of said execute block instruction *[The displacement parameter of an echo instruction*

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*specifies the location of the set of instructions relative to the echo instruction; column 12, lines 20-30].*

17. Referring to claim 5, Fraser has taught the apparatus as claimed in claim 1, comprising a program counter register operable to store an address indicative of a memory location of a program instruction being executed within said sequence of program instructions *[The program counter stores a pointer indicating the next instruction to be executed; column 12, lines 5-7].*

18. Referring to claim 6, Fraser has taught the apparatus as claimed in claim 1, comprising a block counter register operable to store a block count value indicative of a location of a program instruction being executed within said block of two or more program instructions *[The count module stores the length parameter (i.e. block count value) of the echo instruction to determine the remaining instructions in the set of instructions (i.e. location of a program instruction being executed within the block); column 12, lines 32-40].*

19. Referring to claim 7, Fraser has taught the apparatus as claimed in claim 5, wherein when executing said block of two or more program instructions, said program counter registers stores an address indicative of a memory location of said execute block instruction *[the address of an instruction within the set of instructions]* and said block counter register stores a block count value indicative of said program instruction location of a program instruction being executed within said block of two or more program instructions *[the count of remaining instruction in the set of instruction]* corresponding to said execute block instruction *[column 12, lines 14-37].*

20. Referring to claim 10, Fraser has taught the apparatus as claimed in claim 2, wherein upon completion of execution of said block of two or more program instructions said instruction decoder is operable to return processing to a program instruction following said execute block instruction as indicated by said program counter register *[Upon completion of the set of instructions the program counter is restored and the processing is restored to a program instruction following the echo instruction as indicated by the program counter; column 12, lines 37-44].*

21. Referring to claim 11, Fraser has taught a method for processing data, said method comprising the steps of:

fetching program instructions from a sequence of memory locations with an instruction fetching circuit *[access module; Fig. 3, component 332; column 11, line 65 – column 12, line 3];*

controlling data processing operations specified by said program instructions with an instruction decoder *[evaluate module; Fig. 3, component 334; column 12, lines 3-13];* and

executing said data processing operations with an execution circuit controlled by said instruction decoder *[execute module; Fig. 3, component 338; column 12, lines 7-13];*

wherein said instruction decoder is responsive to an execute block instruction *[echo instruction]* to trigger fetching of a block of two or more program instructions *[set of instructions]* by said instruction fetching circuit and execution of said block of two or more program instructions by said execution circuit, said block of two or more



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instructions containing a number of program instructions specified by a block length field *[length parameter]* within said executed block instruction and being stored at a memory location specified by a location field *[displacement parameter]* within said execute block instruction *[When the evaluate module determines there is an echo instruction it triggers the fetching and execution of a set of instructions, whose number and location are indicated by the length and displacement parameters, respectively, of the echo instruction; column 12, lines 14-44].*

22. Referring to claim 12, given the similarities between claim 2 and claim 12 the arguments as stated for the rejection of claim 2 also apply to claim 12.

23. Referring to claim 13, given the similarities between claim 3 and claim 13 the arguments as stated for the rejection of claim 3 also apply to claim 13.

24. Referring to claim 14, given the similarities between claim 4 and claim 14 the arguments as stated for the rejection of claim 4 also apply to claim 14.

25. Referring to claim 15, given the similarities between claim 5 and claim 15 the arguments as stated for the rejection of claim 5 also apply to claim 15.

26. Referring to claim 16, given the similarities between claim 6 and claim 16 the arguments as stated for the rejection of claim 6 also apply to claim 16.

27. Referring to claim 17, given the similarities between claim 7 and claim 17 the arguments as stated for the rejection of claim 7 also apply to claim 17.

28. Referring to claim 20, given the similarities between claim 10 and claim 20 the arguments as stated for the rejection of claim 10 also apply to claim 20.

29. Referring to claim 21, Fraser has taught a computer program product including

a computer program operable to control a data processing apparatus having  
an instruction fetching circuit *[access module; Fig. 3, component 332]*  
operable to fetch program instructions from a sequence of memory locations  
*[column 11, line 65 – column 12, line 3],*

an instruction decoder *[evaluate module; Fig. 3, component 334]*  
responsive to program instructions fetched by said instruction fetching circuit to  
control data processing operations specified by said program instructions  
*[column 12, lines 3-13], and*

an execution circuit *[execute module; Fig. 3, component 338]* operable  
under control of said instruction decoder to execute said data processing  
operations *[column 12, lines 7-13];*

said computer program including one or more an execute block  
instructions *[echo instruction]* operable to trigger fetching of a block of two or  
more program instructions *[set of instructions]* by said instruction fetching circuit  
and execution of said block of two or more program instructions by said  
execution circuit, said block of two or more instructions containing a number of  
program instructions specified by a block length field *[length parameter]* within  
said executed block instruction and being stored at a memory location specified  
by a location field *[displacement parameter]* within said execute block instruction  
*[When the evaluate module determines there is an echo instruction it triggers the  
fetching and execution of a set of instructions, whose number and location are*

*indicated by the length and displacement parameters, respectively, of the echo instruction; column 12, lines 14-44].*

30. Referring to claim 22, given the similarities between claim 2 and claim 22 the arguments as stated for the rejection of claim 2 also apply to claim 22.

31. Referring to claim 23, given the similarities between claim 3 and claim 23 the arguments as stated for the rejection of claim 3 also apply to claim 23.

32. Referring to claim 24, given the similarities between claim 4 and claim 24 the arguments as stated for the rejection of claim 4 also apply to claim 24.

33. Referring to claim 25, given the similarities between claim 5 and claim 25 the arguments as stated for the rejection of claim 5 also apply to claim 25.

34. Referring to claim 26, given the similarities between claim 6 and claim 26 the arguments as stated for the rejection of claim 6 also apply to claim 26.

35. Referring to claim 27, given the similarities between claim 7 and claim 27 the arguments as stated for the rejection of claim 7 also apply to claim 27.

36. Referring to claim 30, given the similarities between claim 10 and claim 30 the arguments as stated for the rejection of claim 10 also apply to claim 30.

### ***Claim Rejections - 35 USC § 103***

37. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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38. Claims 8-9, 18-19, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fraser.

39. Referring to claim 8,

Fraser has taught the apparatus as claimed in claim 6.

Fraser has not explicitly taught an exception handling circuit operable upon occurrence of an exception during execution of said block of two or more instructions to store said block count value and upon completion of handling of said exception to restart execution of said block of two or more program instructions at a program instruction within said block of two or more instructions indicated by said block count value.

However, Examiner takes Official Notice that exception handling circuits that save a processor's execution state upon occurrence of an exception and restart execution at the program instruction indicated by the saved execution state upon completion of handling the exception are conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to included an exception handling circuit that saves the processor's execution state, which in the instant case includes a block count value, upon occurrence of an exception and restarts execution at the program instruction indicated by the saved state, including the block count value, upon completion of handling the exception since doing so allows the processor to properly resume execution of a program after an exception.

40. Referring to claim 9,

Fraser has taught the apparatus as claimed in claim 6.

Fraser has not explicitly taught an exception handling circuit operable to store an address of said execute block instruction upon occurrence of an exception and to restore said address of said execute block instruction to said program counter register upon said completion of handling of said exception.

However, Examiner takes Official Notice that exception handling circuits that save a processor's execution state upon occurrence of an exception and restore the saved execution state upon completion of handling the exception are conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an exception handling circuit that saves the processor's execution state, which in the instant case includes a program counter that, when the execute block instruction is going to execute, contains the address of the block execute instruction, upon occurrence of an exception and restores the saved state, including the program counter, upon completion of handling the exception since doing so allows the processor to properly resume execution of a program after an exception.

41. Referring to claim 18, given the similarities between claim 8 and claim 18 the arguments as stated for the rejection of claim 8 also apply to claim 18.

42. Referring to claim 19, given the similarities between claim 9 and claim 19 the arguments as stated for the rejection of claim 9 also apply to claim 19.

43. Referring to claim 28, given the similarities between claim 8 and claim 28 the arguments as stated for the rejection of claim 8 also apply to claim 28.

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44. Referring to claim 29, given the similarities between claim 9 and claim 29 the arguments as stated for the rejection of claim 9 also apply to claim 29.

### ***Conclusion***

45. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib  
Examiner  
Art Unit 2181

*Supervisor*  
*Fritz Fleming*  
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